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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,790	05/28/2004	Wen-Long Chin	ADMP0003USA	3789

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EXAMINER	
KIM, KENNETH S	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,790	CHIN, WEN-LONG	
	Examiner	Art Unit	
	Kenneth S. KIM	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-12 are presented for examination.

2. The abstract of the disclosure is objected to because the current abstract does not reflect the inventive feature of the claimed invention to distinguish over the prior art. Correction is required. See MPEP § 608.01(b).

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant failed to adequately teach how to make and use a multiplexer with two outputs, and it would require a person of ordinary skill in the art undue experimentation to develop and control such a means.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 7, it is not clear how the multiplexer is controlled to select two outputs.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Asato, U.S. Patent No. 6,145,074.

Asato teaches the invention as claimed in claim 1 including a very long instruction word (VLIW) architecture comprising:

(a) a VLIW input port for sequentially inputting a plurality o VLIWs, each VLIW comprising a plurality of instructions' (col. 6, line 39),

(b) a decoder for decoding the instructions of the VLIWs (col. 1, line 27),

(c) at Least a register for storing data (1),

(d) a plurality of data buses for sending data (22),

(e) a plurality of arithmetic logic units (ALUs) for executing the instructions of the VLIWs (21),

(f) a plurality of multiplexers, each output port of the multiplexers being connected to an input port of one of the corresponding ALUS, and each input port of the multiplexers being connected to the register and output ports of the ALUS via the data buses (72,73), wherein each of the multiplexers selects two outputs from outputs of the register and the ALUS to send to the corresponding ALU so that the corresponding ALU executes one of the instructions to operate the two selected outputs (3, 4), and

further teaches as in claims 2-6,

(g) multiplexer selects the output according to instruction decoder signal (col. 1, line 28; col. 5, line 66) – claim 2,

(h) periodically executes instructions in VLIW according to schedule flag (cycle bit in VLIW) – claims 3 and 4,

(i) decoder receives VLIW via input port from instruction register (decoder receives instruction from instruction register) – claim 5, and

(j) multiplexer selects an output from ALU to store in register (data to be stored in register can be obtained from any available source such as a multiplexer) – claim 6.

The VLIW architecture apparatus claims 7-12 are equivalently rejected based on the same reason.

9. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi, U.S. Patent No. 5,805,852.

Nakanishi teaches the invention as claimed in claim 1 including a very long instruction word (VLIW) architecture comprising:

(a) a VLIW input port for sequentially inputting a plurality o VLIWs, each VLIW comprising a plurality of instructions' (col. 8, line 57),

(b) a decoder for decoding the instructions of the VLIWs (3),

(c) at least a register for storing data (5),

(d) a plurality of data buses for sending data (11),

(e) a plurality of arithmetic logic units (ALUs) for executing the instructions of the VLIWs (7),

(f) a plurality of multiplexers, each output port of the multiplexers being connected to an input port of one of the corresponding ALUS, and each input port of the multiplexers being connected to the register and output ports of the ALUS via the data buses (provides inputs to L1 and L2), wherein each of the multiplexers selects two outputs from outputs of the register and the ALUS to send to the corresponding ALU so that the corresponding ALU executes one of the instructions to operate the two selected outputs (L1, L2), and

further teaches as in claims 2-6,

(g) multiplexer selects the output according to instruction decoder signal (col. 9, line 20) – claim 2,

(h) periodically executes instructions in VLIW according to schedule flag (cycle bit in VLIW) – claims 3 and 4,

(i) decoder receives VLIW via input port from instruction register (decoder receives instruction via instruction register from cache) – claim 5, and

(j) multiplexer selects an output from ALU to store in register (data to be stored in register can be obtained from any available source such as a multiplexer) – claim 6.

The VLIW architecture apparatus claims 7-12 are equivalently rejected based on the same reason.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakhin et al taught a method of executing VLIW instructions using register bypass multiplexers.

Nickolls taught a method of providing operand data directly from execution units.

Balmer et al taught a method of providing result data directly to execution units.

Macri et al taught a method of using cycle bits in VLIW instructions.

Wang et al taught a method of bypassing register file for a plurality of ALUs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

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KENNETH S. KIM
PRIMARY EXAMINER